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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,168	03/24/2004	Hiroaki Inoue	Q80602	6480

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SUGHRUE MION, PLLC  
2100 PENNSYLVANIA AVENUE, N.W.  
SUITE 800  
WASHINGTON, DC 20037

EXAMINER
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GUYTON, PHILIP A

ART UNIT	PAPER NUMBER
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2113

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/807,168

Applicant(s)

INOUE ET AL.

Examiner

Philip Guyton

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date See Continuation Sheet.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :20040324,20041029,20060210,20061106.

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Specification***

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Rejections - 35 USC § 101***

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 20-35 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Independent claims 20, 21, and 22 recite "a parallel processing program" which is not a process, machine, manufacture, or composition of matter as required by 35 U.S.C. 101. It is suggested that the program be stored on a computer-readable medium in order to realize its functionality.

### ***Double Patenting***

4. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

5. Claims 1-35 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-42 of copending Application No. 10/390595, and claims 1-45 of copending Application No. 11/080730. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

### ***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(f) he did not himself invent the subject matter sought to be patented.

7. Claims 1-35 are rejected under 35 U.S.C. 102(f) because the applicant did not invent the claimed subject matter. Claims 1-7, 10-16, 19-26, 29-32, and 35 recites identical subject matter as in copending Application No. 10/390595. Additionally, claims 8, 9, 17, 18, 27, 28, 33, and 34 recite the same invention as claimed in copending Application No. 11/080,730. Each of these applications maintain different inventive entities.

8. The issue of priority under 35 U.S.C. 102(f) of this single invention must be resolved.

Since the U.S. Patent and Trademark Office normally will not institute an interference between applications or a patent and an application of common ownership (see MPEP Chapter 2300), the assignee is required to state which entity is the prior inventor of the conflicting subject matter. A terminal disclaimer has no effect in this situation since the basis for refusing more than one patent is priority of invention under 35 U.S.C. 102(f) or (g) and not an extension of monopoly.

Failure to comply with this requirement will result in a holding of abandonment of this application.

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

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granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-35 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S.

Patent Application Pub. No. 2003/0182355 to Edahiro et al. (hereinafter Edahiro).

The applied reference has a common assignee with the instant application.

Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claim 1, Edahiro discloses a parallel processing system by an OS for single processors which

operates an OS for single processors and an application on a multiprocessor (paragraph 12), and

controls a unit of work that can be parallelized within said application operating on one processor as a new unit of work on other processor, thereby conducting parallel processing by said multiprocessor with respect to said application (paragraphs 14,16).

With respect to claim 2, Edahiro discloses a parallel processing system by an OS for single processors which

operates an OS for single processors and an application on a multiprocessor (paragraph 12),

said multiprocessor being logically divided into two groups of a first processor side and a second processor side (paragraph 15), and

controls a unit of work that can be parallelized within said application operating on a processor on said first processor side as a new unit of work on a processor on said second processor side, thereby conducting parallel processing by said multiprocessor with respect to said application (paragraph 14,16).

With respect to claim 3, Edahiro discloses a parallel processing system by an OS for single processors which

operates an OS for single processors and an application on a multiprocessor (paragraph 32),

said multiprocessor being divided into two groups of a first processor side and a second processor side (paragraph 33),

operates said OS for single processors and said application on a processor on said first processor side (paragraph 34), and

controls a unit of work that can be parallelized within said application as a new unit of work on a processor on said second processor side, thereby conducting parallel processing by said multiprocessor with respect to said application (paragraph 35).

With respect to claim 4, Edahiro discloses wherein the unit of work that can be parallelized within said application is created in advance on a processor on said second processor side (paragraph 17).



With respect to claim 5, Edahiro discloses wherein the unit of work that can be parallelized within said application is created and activated as a new unit of work on a processor on said second processor side (paragraph 18).

With respect to claim 6, Edahiro discloses wherein said OS for single processors having a virtual memory mechanism is mounted on the processor on said first processor side and each processor on said second processor side (paragraph 19).

With respect to claim 7, Edahiro discloses wherein the new unit of work on the processor on said second processor side is controlled synchronously or asynchronously with the unit of work on the processor on said first processor side (paragraph 20).

With respect to claim 8, Edahiro discloses wherein synchronous processing and data transmission and reception are enabled between units of work on the processor on said first processor side and on the processor on said second processor side (paragraph 214).

With respect to claim 9, Edahiro discloses wherein an inter-process communication unit which executes synchronous processing and data transmission and reception between said units of work by a semaphore system and a message queue system is provided on the processor on said first processor side and on the processor on said second processor side (paragraphs 222-242).

With respect to claim 10, Edahiro discloses wherein a parallel processing unit which conducts control related to the unit of work including said creation of the unit of work and an OS service unit which provides service of said OS for single processors to

said unit of work are incorporated into each of said first processor side and said second processor side (paragraph 21).

With respect to claim 11, Edahiro discloses a control processing relay unit which conducts transmission and reception of a control signal and data between said first processor side and said second processor side (paragraph 22).

With respect to claim 12, Edahiro discloses wherein said control processing relay unit includes an interruption control device corresponding to each processor and a communication region corresponding to each processor,

said interruption control device being formed of an interruption instruction unit which instructs other processor to interrupt, an interruption state holding

unit which holds information that an interruption is made by an interruption instruction and an interruption cancellation unit which clears an interruption, and said communication region being formed of a communication reason holding region which holds a communication reason from a communication source processor, a communication data holding region which holds communication data to be communicated and a mutual exclusive control region which locks a communication region to ensure communication (paragraphs 23-25).

With respect to claim 13, Edahiro discloses wherein said control processing relay unit includes an interruption control device corresponding to each processor and a communication region corresponding to each processor,

said interruption control device being formed of an interruption instruction unit which instructs other processor to interrupt, an interruption state holding unit which

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holds information that an interruption is made by an interruption instruction and an interruption cancellation unit which clears an interruption, and

said communication region being formed of a communication queue which holds a communication reason from a communication source processor and communication data to be communicated and a mutual exclusive control region which locks a communication region to ensure communication (paragraphs 26-28).

With respect to claim 14, Edahiro discloses wherein a proxy unit is provided on said first processor side, which is associated with the unit of work on said second processor side by a processing unit number to conduct notification of various kinds of control signals between the unit of work on said second processor side and said OS for single processors (paragraph 29).

With respect to claim 15, Edahiro discloses wherein said parallel processing unit, the OS service unit, the control processing relay unit and the proxy unit are incorporated in a modular fashion (paragraph 30).

With respect to claim 16, Edahiro discloses wherein said parallel processing unit on said second processor side is provided with a function of creating a unit of work to be parallel-processed by other processor on said second processor side (paragraph 31).

With respect to claim 17, Edahiro discloses wherein each said processor is mounted with said OS for single processors having a virtual memory mechanism to enable synchronous processing and data transmission and reception between the units of work on said one processor and said other processor (paragraph 214).

With respect to claim 18, Edahiro discloses wherein an inter-process communication unit which executes synchronous processing and data transmission and reception between said units of work by a semaphore system and a message queue system is provided on each said processor (paragraphs 222-242).

With respect to claim 19, Edahiro discloses a control processing relay unit which conducts transmission and reception of a control signal and data at the time of synchronous processing and data transmission and reception between said units of work on each said processor (paragraph 215).

Claims 20-35 are a parallel processing program for operating the parallel processing system of claims 1-19, and are rejected under the same rationale.

### ***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Philip Guyton whose telephone number is (571) 272-3807. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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*Robert M. Bausch*  
ATTORNEY AT LAW  
1500 K STREET, N.W.  
WASHINGTON, D.C. 20004  
202-462-2100